IN THE SPECIFICATION:

Please replace paragraphs [0021] – [0025], as filed, with the following amended paragraphs:

[0021] The invention can be incorporated within a metallization process sequence such as that shown in FIG. 5. The process sequence ~~700~~ of FIG. 5 illustrates ~~several~~ steps 502-506 in the formation of a metallization structure in a high aspect ratio feature. ~~In step 701, a~~ A high aspect ratio feature, *e.g.*, a trench or via, is formed on a substrate such as a semiconductor wafer. The trench or via may be formed by conventional lithographic and etching techniques in an insulating layer that has previously been deposited on the wafer. ~~In step 703, a~~ A barrier layer is deposited inside the high aspect ratio feature. The barrier layer, which prevents undesirable diffusion between the underlying substrate and a subsequently deposited metal layer, can be deposited either by chemical vapor deposition (CVD) or physical vapor deposition (PVD). Optionally, an adhesion layer may also be deposited (not shown in FIG. 5) prior to the formation of the barrier layer.

[0022] A seed layer of metal is then deposited, by CVD or PVD, on the barrier layer ~~in step 705~~. This metal seed layer is typically relatively thin, and is used to facilitate a subsequent electrochemical deposition (or electroplating) performed in steps 502-506 ~~707~~. The seed layer metal may be the same as the metal to be deposited in steps 502-506 ~~707~~, or another conductive material such as metal nitride, among others. For example, in copper applications, the seed layer may be copper. However, other metals or conductive materials suitable for promoting electroplating can also be used. For example, noble metals or highly conductive metals such as gold, silver, platinum, palladium, nickel, aluminum, tungsten, tin or their alloys are appropriate. When conductive nitrides are used, such as tungsten nitride ~~is used~~, the nitride layer may also act as a barrier layer.

[0023] During steps 502-506 ~~707~~, electrochemical plating is performed using a plating solution to deposit a metal layer to a thickness that is at least sufficient to

substantially fill the high aspect ratio feature. According to embodiments of the invention, the high aspect ratio feature is filled with the metal in a void-free and seam-free manner by pulse plating techniques using modulated waveforms. In one aspect of the invention, the modulated waveforms comprise electrical pulses of opposite polarities, along with time intervals of zero electrical pulses, or "off-times". The off-times in the plating waveforms allow re-distribution of various chemical species in the plating solution around the high aspect ratio feature to achieve desirable deposition profiles.

[0024] The metal is deposited by sequentially applying an electrodeposition pulse (step 502) followed by an electrodissolution pulse (step 504) to the substrate. After each electrodissolution pulse and before the next electrodeposition pulse, there is provided at least one time interval of zero electrical voltage or current, also known as an "off-time", between the pulses. The first two electrodeposition pulses should preferably have the same time durations. Thereafter, the time durations of subsequent electrodeposition pulses are gradually decreased to provide a void-free and seam-free deposition of metal in high aspect ratio features, as may be conducted in step 506.

[0025] After the formation of the metal layer to a desired thickness, a planarization step ~~709~~ may be performed to remove portions of the metal layer that lie outside the high aspect ratio feature, resulting in a planarized metallization structure on the wafer. The planarization may be performed, for example, by chemical mechanical polishing (CMP).

Please replace paragraphs [0034] – [0037], as filed, with the following amended paragraphs:

[0034] FIG. [[4]] 3 is a schematic diagram showing the electrical connections for an electroplating system according to embodiments of the invention. A power supply [[402]] 302 is connected to two electrodes [[404]] 304 (*e.g.*, anode) and [[406]] 308 (*e.g.*, cathode) of an electroplating system. The cathode [[406]] 308 electrically contacts a seed layer [[410]] 310 on the plating surface [[408]] 306 of the substrate [[430]] 330. The power supply [[402]] 302 preferably includes a control circuit [[420]] (not shown) that switches between a constant current operation and a constant voltage

operation. The control circuit [[420]] of the power supply [[402]] 302 also controls the polarity of the output.

[0035] The power supply [[402]] 302 preferably also includes a switching circuit [[422]] (not shown) that is programmable to produce a variety of output waveforms, such as an output waveform comprising combinations of a constant voltage or current output for a first duration, a constant voltage or current output for a second duration, and an "off-time" corresponding to zero voltage or current output. The invention contemplates utilizing a variety of power supply designs that are capable of producing such output waveforms and is not limited to any particular power supply design.

[0036] According to embodiments of the invention, pulse plating is used in conjunction with provisions of an "off-time", to control the electrodeposition and electrodissolution of metal in the vicinity of the high aspect ratio structure. Although the present discussion focuses on the effect around a high aspect ratio feature, it is recognized that the off-time may also affect metal deposition and dissolution in other areas of the substrate. In pulse plating, electrical pulses - either voltage or current pulses, are applied to the substrate [[430]] 330 in certain combinations. These pulse combinations may comprise different sequences of pulses of different polarities to achieve metal deposition or metal dissolution. This contrasts with DC plating, in which a continuous voltage or current is applied to the substrate for a time duration for metal deposition.

[0037] FIG. 4 illustrates a pulse plating waveform having current pulses with different polarities. In this example, current pulses ~~511 and 513~~ I_d correspond to electrodeposition pulses, during which copper ions in the electrolyte are accelerated towards the cathode [[406]] 306, resulting in the plating of copper on the substrate [[430]] 330. The negative current pulses ~~521 and 523~~ V_r correspond to electrodissolution pulses, during which the copper that has been plated on the substrate [[430]] 330 is dissolved by being converted into copper ions in the electrolyte. By using different combinations of electrical pulses of opposite polarities, plating of copper can be achieved with varying profiles. To achieve superfill in a high aspect ratio structure, *e.g.*, a via or trench, it is desirable to have a higher current density at the bottom than at the top of the structure.